High-Voltage Wordline Generator for Low-Power Program Operation in NAND Flash Memories

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***Abstract*— High-voltage wordline generation circuit with stage-controlled charge pump is developed for low-power NAND flash memories. The proposed stage-controlled charge pump controls an optimized number of stages according to the required program voltage. The proposed high-voltage generator provides sleep-mode operation by turning off the driving clock and regulators during the program verify operation. Using these techniques, the proposed high-voltage generator reduces about 50 percent of power consumption in comparison with a conventional scheme.**

I. Introduction

Recently, NAND flash memories are widely adopted in mobile applications such as a smartphone, tablet PC, MP3 player, digital camera, notebook and so on. Since the battery lifetime is one of the important factors in mobile devices, low-power design must be considered. NAND flash memories receive a single supply voltage such as 3.3V or 1.8V, and high voltages which are required for read, program and erase operations are generated by charge pump circuits inside the chip. Typical NAND flash memory consumes large current during program operation due to the simultaneous operation of several high-voltage generators.

A high-voltage generator consists of a charge pump, a voltage regulator and an oscillator as shown in Fig. 1. NAND flash memory requires the high-voltage generator with wide range output voltage to support staircase linear program operation which enhances the program performance [1], [2]. Since this generator requires high output regulated voltage such as 25V and a fast rising time for an arbitrary load capacitance, the charge pump with the large number of stages and stage capacitor is used [3], [4], [5]. However, the charge pump with large number of stages increases the current consumption and results in poor power efficiency [6]. Also, the voltage regulator draws large current when the generator requires low output regulated voltage for a staircase program pulse.

This paper presents a low-power high-voltage wordline generator which supports a staircase linear program pulse in NAND flash memories. The approach is based on the optimized stage-controlled charge pump according to the output regulated voltage range. A sleep-mode operation is also proposed to inhibit unnecessary generator operation during non-program pulse period. The proposed schemes are implemented on a 64-Gb MLC NAND flash memory fabricated with a 20nm technology.

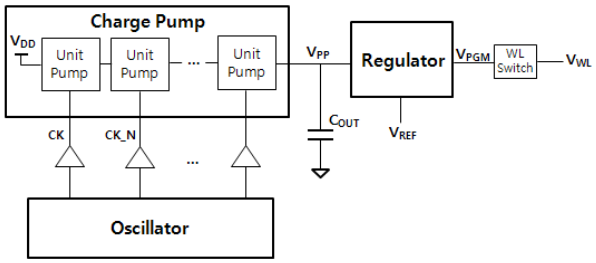

Fig. 1. Block diagram of a conventional high-voltage generation circuit

II. High-Voltage Wordline Generator

Fig. 2 shows the proposed high-voltage wordline generator circuit. It consists of a stage-controlled charge pump, a stage control circuit, a ring oscillator and regulators. The output of high-voltage generator drives a selected wordline through a switch circuit during the program operation in NAND flash memory. The charge pump with a number of pump stages elevates a supplied voltage to a higher voltage, where the unit stage is composed of a stage capacitor and switching elements [3], [5]. The ring oscillator generates periodic clock and drives stage capacitors in the charge pump. The regulator limits the pump output voltage to a required voltage. The Regulator consists of a switching regulator and a linear regulator. The output from a switching regulator becomes the input of a linear regulator. A switching regulator [7] is composed of a resistive divider and a comparator, where the comparator detects whether the divided voltage is higher or not than a reference level and acts as on/off switch. Since the switching regulator switches the driving clock of the charge pump, the output ripple voltage is hard to avoid and it affects on a programmed cell distribution to be widen. A linear regulator [8], [9] consists of a resistive divider, an operational amplifier and an active device such as a PMOS transistor. The linear regulator has an advantage of low output ripple voltage but it consumes large power when the difference between input voltage and output voltage, called *drop-out voltage*, is increased. To obtain more stable and higher power efficiency, combined regulators are used in parallel. Stage control circuit consists of D-latches and

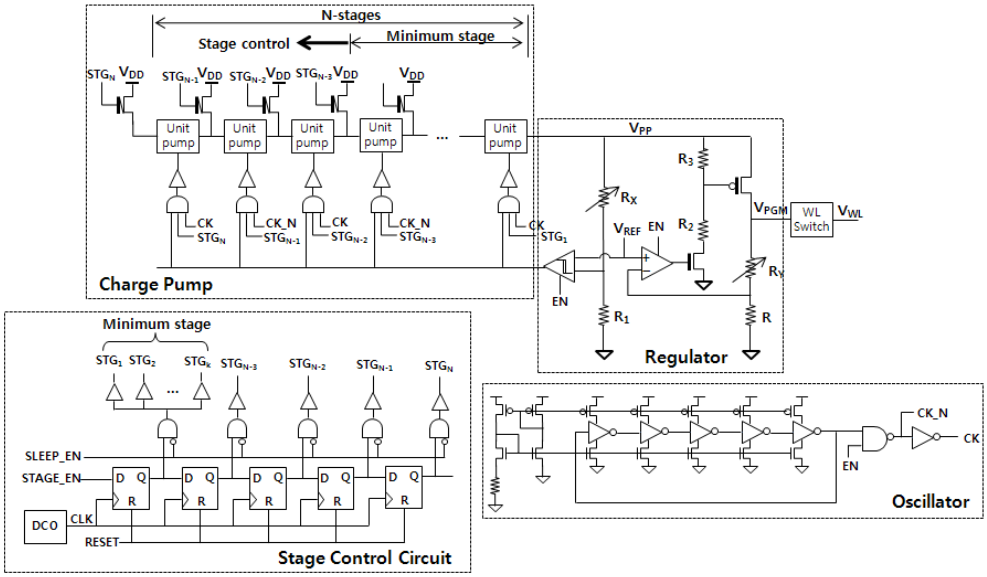

Fig. 2. Schematic of the proposed high-voltage wordline generator

the digitally-controlled oscillator (DCO). Stage control circuit creates stage control signals STG_i $(i = 1, 2, ..., N-1, N)$, where STG_i signals limit the clock input of unit pump and supplied voltage to the charge pump through the high-voltage NMOS transistor.

III. Low-Power Technique

A. Stage-controlled Charge Pump Scheme

During the program operation, NAND flash memory requires high-voltage with a wide output range such as from 10V to 30V. Typically, the output voltage of the charge pump [3], [6] can be expressed by

$$V_{PP} = (N+1)V_g - \frac{NI_{OUT}}{f(C+C_S)} \tag{1}$$

where N is the number of stages, V_g is maximum gain per unit pump stage, I_{OUT} is output load current, f is clock frequency, C is stage capacitance, and C_S is the parasitic capacitance in the pump stage. A high-voltage generator can be modeled as shown in Fig. 3(a). The output voltage of charge pump can be expressed by a voltage source V_O, an equivalent resistance R_{PP}, and output load current I_{OUT} as same as Eq. (1) . Also, the output voltage of regulator can be expressed by

$$V_{PGM} = V_{PP} - I_{OUT} \cdot R_{REG} \tag{2}$$

where R_{REG} is the equivalent resistance of regulator.

Fig. 3(b) shows the output voltage curve of charge pump against the output load current at different number of stages. If a required V_{PGM} is the same regulated voltage same as independent of the number of stages N or $(N-1)$, N-stages charge pump requires higher output load current than $(N-1)$. Fig. 3(c) shows an example of the output voltage vs. the output load current curve for the charge pump with various number of stages.

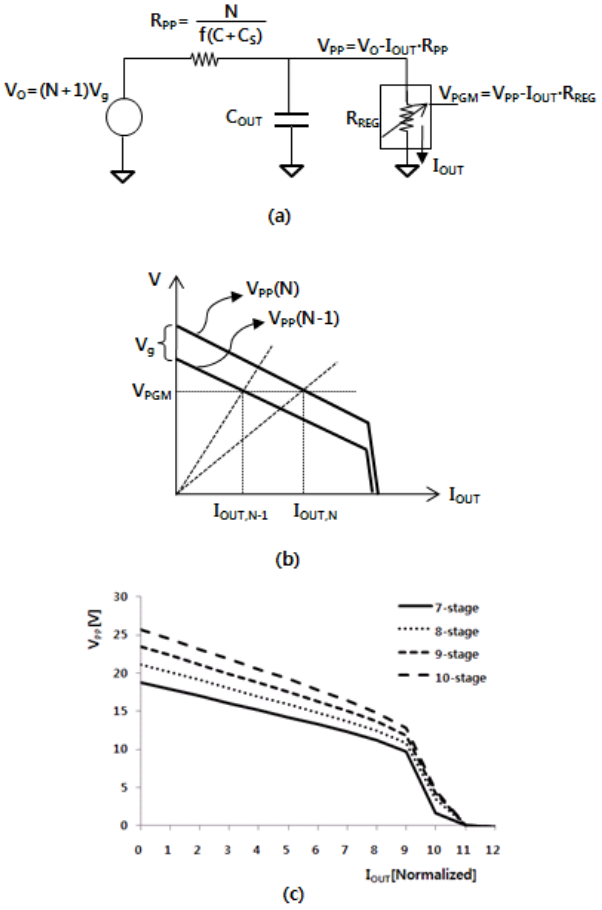

Fig. 3. Equivalent circuit model and I-V curve of the high-voltage generator. (a) equivalent circuit, (b) plot of the output voltage vs. output load current at different number of stages, and (c) an example of I-V curve

Typically, maximum number of stages N_{MAX} are determined by the maximum value of the required program voltage according to Eq. (1). However, the N_{MAX} too large for low voltage generation. Since the current consumption is proportional to the number of stages and output load current [6], the excessive number of stages not only waste the current but also degrade power efficiency.

In order to overcome the large current consumption and poor efficiency, the proposed high-voltage generator controls the number of pump stages depending on the required program voltage. To control the number of stage, the DCO creates periodic clock and D-latches generate stage control signals when the stage enable signal ($STAGE\_EN$) is turned-on. When NAND flash requires low program voltage, the clock controlled by STG_i signals drives only the minimum stage of the charge pump. The output voltage of the charge pump V_{PP} is limited by switching regulator as follows.

$$V_{PP} = V_{REF}\left(1 + \frac{R_X}{R_1}\right) \tag{3}$$

The stage-controlled signals STG_i are sequentially turned on according to the required program voltage increased by staircase manner. The linear low-dropout regulator generates program voltage V_{PGM} applied to a wordline. The staircase program voltage is obtained by increasing the resistance of R_Y and the voltage step ΔV_{PGM} determined by a fixed amount of the resistance ΔR_Y is equal to

$$\Delta V_{PGM} = V_{REF}\frac{\Delta R_Y}{R} \tag{4}$$

The Fig. 4(a) shows the simulation results of the stage-controlled charge pump scheme.

B. Sleep Mode Operation

In NAND flash memories, the program operation is composed of the several numbers of program pulses and verify steps, where the verify step checks whether threshold voltage of the cell (Vth) reaches the required level or not. The verify step operates between the staircase high voltage program pulses as shown in Fig 4(b). Since a verify operation uses a low voltage range compared with the program voltage, a different voltage generator supplies the verify voltage. In addition, if the output voltage V_{PP} is discharged during program verify step, the high-voltage generator requires both time and current to recover previous voltage. Therefore, conventional scheme works both high-voltage wordline generator and verify generator simultaneously during program verify step although it does not need high voltage. To reduce the power consumption in the high-voltage generator, sleep-mode operation is proposed during in between program pulse steps. The sleep mode cuts the current path on the output load in Eq. (1) after a program pulse. Therefore, the high-voltage generator stops driving the clock for the charge pump and disables regulators to eliminate the output current except the leakage current. If there is no leakage current, recovery time and current are small. The sleep mode is released before the next program pulse is applied to a wordline as short timing overhead for re-activation shown in Fig. 4(b).

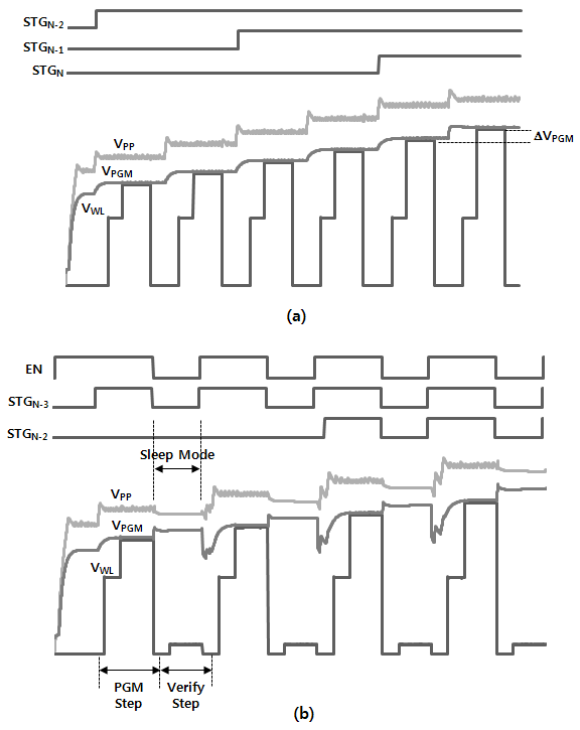

Fig. 4. Timing diagram of (a) stage-controlled charge pump scheme and (b) sleep-mode operation scheme

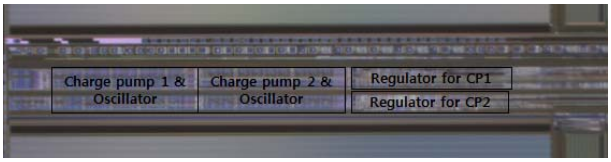

Fig. 5. Microphotograph of the wordline high voltage generator

IV. Experimental Results

The proposed high-voltage generator for a wordline is fabricated in a 20nm technology. There are two high-voltage generators as shown in Fig 5. The charge pump 1 (CP1) is for non-programmed wordlines and the other (CP2) is for a programmed wordline. The stage-controlled charge pump is applied for a programmed wordline high-voltage generator, where the number of stages varies.

Fig. 6 shows the measured current and voltage waveforms during the program operation. Fig. 6 compares current consumption between conventional and proposed scheme with stage-controlled charge pump and sleep mode operation. Conventional scheme activates all pump stages, the switching regulator are deactivated, (*i.e.* driving clock is always activated) and the linear regulator works. The peak current happens at the rising edge of V_{PP}. Conventional scheme consumes current at least more than 2 times compared with the proposed scheme because it requires higher output load current to create the

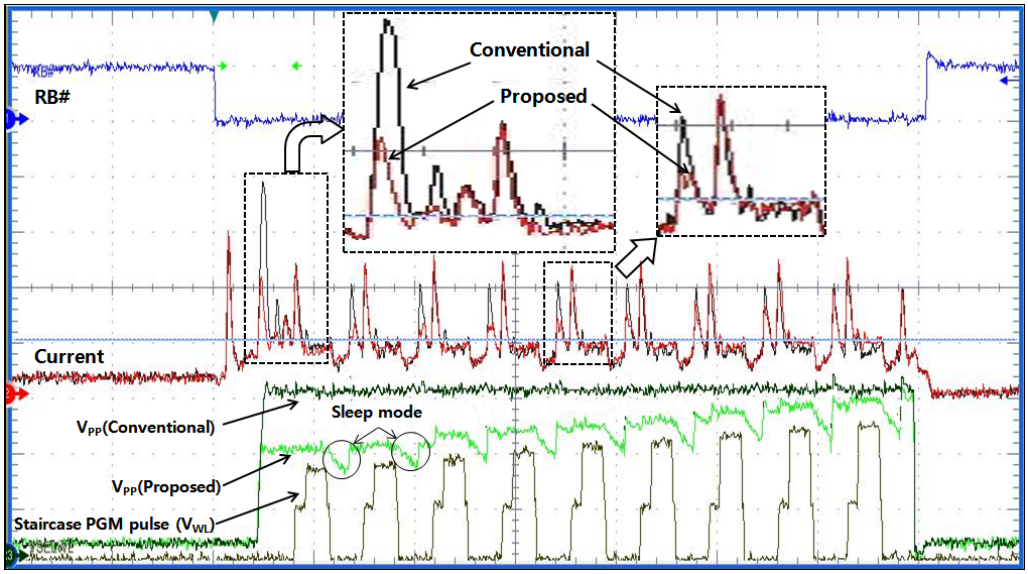

Fig. 6. Measured current and voltage waveform during program operation

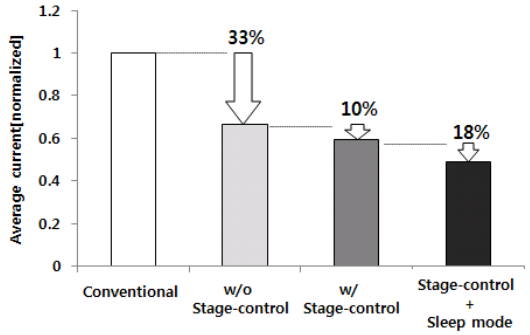

Fig. 7. Current reduction between conventional and proposed schemes

same V_{PGM}. As the V_{PP} difference between conventional and proposed scheme decreases, the gap of current consumption is reduced because charge pump and regulators operate as similar condition. In the Fig. 6, the V_{PP} (Proposed) decreases during sleep-mode operation because of probing leakage from measurement environment.

Fig. 7 shows the average current consumption with the conventional and proposed high-voltage generating schemes. The combined regulation scheme without stage-controlled charge pump reduces 33% compared with conventional scheme. When the stage-controlled charge pump is applied, the average current is decreased to around 10%. When the proposed high-voltage generator works both stage-controlled charge pump and sleep-mode operation, the average current is reduced by around 50% compared with the conventional scheme.

V. Conclusion

The high-voltage wordline generator for low-power operation is implemented in a 20nm technology. The stage-optimized charge pump with variable pump stages is proposed to achieve current reduction and high power efficiency. Also, the proposed generator adopts sleep-mode operation which disables the clock drivers and regulators during in-between program pulses. The results show the proposed schemes reduce the half of the current consumption. This scheme is also available to apply another high voltage generator for non-programmed wordlines in NAND flash memories.

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